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**2-WIRE CMOS SERIAL E<sup>2</sup>PROM**
**S-24CS64A**


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The S-24CS64A is a 2-wired, low power and wide range operation 64 K-bit E<sup>2</sup>PROM organized as 8192 words  $\times$  8 bits.

Page write and sequential read are available.

**■ Features**

- Low power consumption    Standby : 5.0  $\mu$ A Max. ( $V_{CC} = 5.5$  V)  
   Read : 0.8 mA Max. ( $V_{CC} = 5.5$  V)
- Operating voltage range    Read : 1.8 to 5.5 V  
   Write : 2.7 to 5.5 V
- Page write : 32 bytes / page
- Sequential read
- Operating Frequency : 400 kHz ( $V_{CC} = 5$  V $\pm$ 10 %)
- Write disable function when power supply voltage is low
- Endurance: 10<sup>6</sup> cycles/word\*1 (at +25°C) write capable,  
   10<sup>5</sup> cycles/word\*1 (at +85°C)  
   \*1. For each address (Word: 8 bits)
- Data retention: 10 years (after rewriting 10<sup>5</sup> cycles/word at +85°C)
- Write protection : 100 %
- Lead-free products

**■ Packages**

Package name	Drawing code		
	Package	Tape	Reel
8-Pin SOP (JEDEC)	FJ008-A	FJ008-D	FJ008-D
8-Pin TSSOP	FT008-A	FT008-E	FT008-E
WLP-8C	HC008-A	HC008-A	HC008-A

**Caution** This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable.

■ Pin Configurations

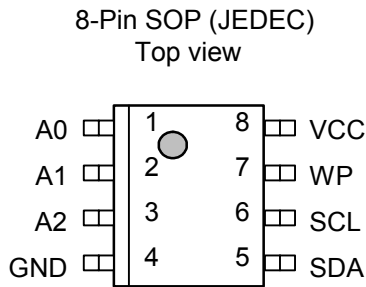


Figure 1

S-24CS64A0I-J8T1G

Table 1

Pin No.	Symbol	Description
1	A0	Slave address input
2	A1	Slave address input
3	A2	Slave address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V <sub>CC</sub> : Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

**Remark** See Dimensions for details of the package drawings.

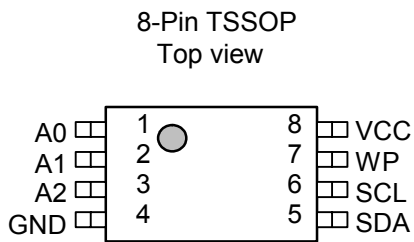


Figure 2

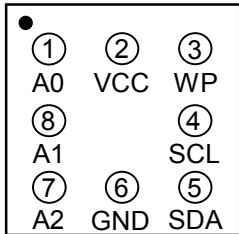
S-24CS64A0I-T8T1G

Table 2

Pin No.	Symbol	Description
1	A0	Slave address input
2	A1	Slave address input
3	A2	Slave address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V <sub>CC</sub> : Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

**Remark** See Dimensions for details of the package drawings.

WLP-8C  
Bottom view



(1.94×1.97×0.6 max.)

Figure 3

S-24CS64A0I-H8T1

Table 3

Pin No.	Symbol	Description
1	A0	Slave address input
2	VCC	Power supply
3	WP	Write protection input Connected to V <sub>CC</sub> : Protection valid Connected to GND: Protection invalid
4	SCL	Serial clock input
5	SDA	Serial data input / output
6	GND	Ground
7	A2	Slave address input
8	A1	Slave address input

**Remark** See Dimensions for details of the package drawings.

■ Block Diagram

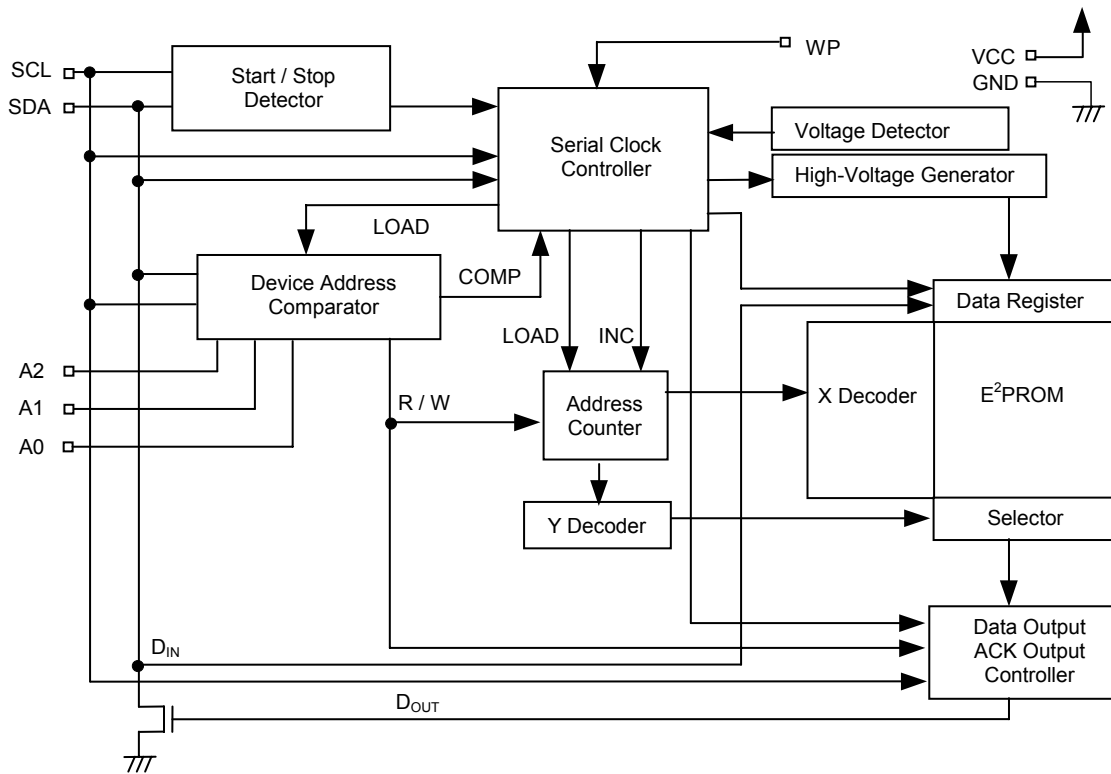


Figure 4

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Ratings	Unit
Power supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Output voltage	V <sub>OUT</sub>	-0.3 to V <sub>CC</sub>	V
Operating ambient temperature	T <sub>opr</sub>	-40 to +85	°C
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Recommended Operating Conditions

Table 5

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V <sub>CC</sub>	Read Operation	1.8	—	5.5	V
		Write Operation	2.7	—	5.5	V
High level input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 2.5 to 5.5 V	0.7×V <sub>CC</sub>	—	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.8 to 2.5 V	0.8×V <sub>CC</sub>	—	V <sub>CC</sub>	V
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 2.5 to 5.5 V	0.0	—	0.3×V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.8 to 2.5 V	0.0	—	0.2×V <sub>CC</sub>	V

## ■ Pin Capacitance

Table 6

(Ta = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V (SCL, A0, A1, A2, WP)	—	—	10	pF
Input/output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V (SDA)	—	—	10	pF

## ■ Endurance

Table 7

Item	Symbol	Operation temperature	Min.	Typ.	Max.	Unit
Endurance	N <sub>W</sub>	-40 to +85°C	10 <sup>5</sup>	—	—	cycles / word*1

\*1. For each address (Word: 8 bits)

■ DC Electrical Characteristics

**Table 8**

Item	Symbol	Conditions	V <sub>CC</sub> = 4.5 to 5.5 V f = 400 kHz			V <sub>CC</sub> = 2.7 to 4.5 V f = 100 kHz			V <sub>CC</sub> = 1.8 to 2.7 V f = 100 kHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I <sub>CC1</sub>	—	—	—	0.8	—	—	0.5	—	—	0.3	mA
Current consumption (WRITE)	I <sub>CC2</sub>	—	—	—	4.0	—	—	3.0	—	—	—	mA

**Table 9**

Item	Symbol	Conditions	V <sub>CC</sub> = 4.5 to 5.5 V			V <sub>CC</sub> = 1.8 to 4.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I <sub>SB</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	—	—	5.0	—	—	3.0	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	—	0.4	—	—	—	V
		I <sub>OL</sub> = 1.5 mA	—	—	0.3	—	—	0.3	V
Current address hold voltage	V <sub>AH</sub>	—	1.5	—	5.5	1.5	—	4.5	V

■ AC Electrical Characteristics

Table 10 Measurement Conditions

Input pulse voltage	0.1×V <sub>CC</sub> to 0.9×V <sub>CC</sub>
Input pulse rising / falling time	20 ns
Output judgement voltage	0.5×V <sub>CC</sub>
Output load	100 pF+ Pull-up resistor 1.0 kΩ

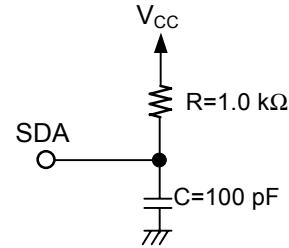


Figure 5 Output Load Circuit

Table 11

Item	Symbol	V <sub>CC</sub> = 4.5 to 5.5 V			V <sub>CC</sub> = 3.0 to 4.5 V			V <sub>CC</sub> = 1.8 to 3.0 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f <sub>SCL</sub>	0	—	400	0	—	400	0	—	100	kHz
SCL clock time “L”	t <sub>LOW</sub>	1.0	—	—	1.0	—	—	4.7	—	—	μs
SCL clock time “H”	t <sub>HIGH</sub>	0.9	—	—	0.9	—	—	4.0	—	—	μs
SDA output delay time	t <sub>AA</sub>	0.1	—	0.9	0.1	—	0.9	0.1	—	3.5	μs
SDA output hold time	t <sub>DH</sub>	50	—	—	50	—	—	100	—	—	ns
Start condition setup time	t <sub>SU.STA</sub>	0.6	—	—	0.6	—	—	4.7	—	—	μs
Start condition hold time	t <sub>HD.STA</sub>	0.6	—	—	0.6	—	—	4.0	—	—	μs
Data input setup time	t <sub>SU.DAT</sub>	100	—	—	100	—	—	200	—	—	ns
Data input hold time	t <sub>HD.DAT</sub>	0	—	—	0	—	—	0	—	—	ns
Stop condition setup time	t <sub>SU.STO</sub>	0.6	—	—	0.6	—	—	4.0	—	—	μs
SCL • SDA rising time	t <sub>R</sub>	—	—	0.3	—	—	0.3	—	—	1.0	μs
SCL • SDA falling time	t <sub>F</sub>	—	—	0.3	—	—	0.3	—	—	0.3	μs
Bus release time	t <sub>BUF</sub>	1.3	—	—	1.3	—	—	4.7	—	—	μs
Noise suppression time	t <sub>I</sub>	—	—	50	—	—	100	—	—	100	ns

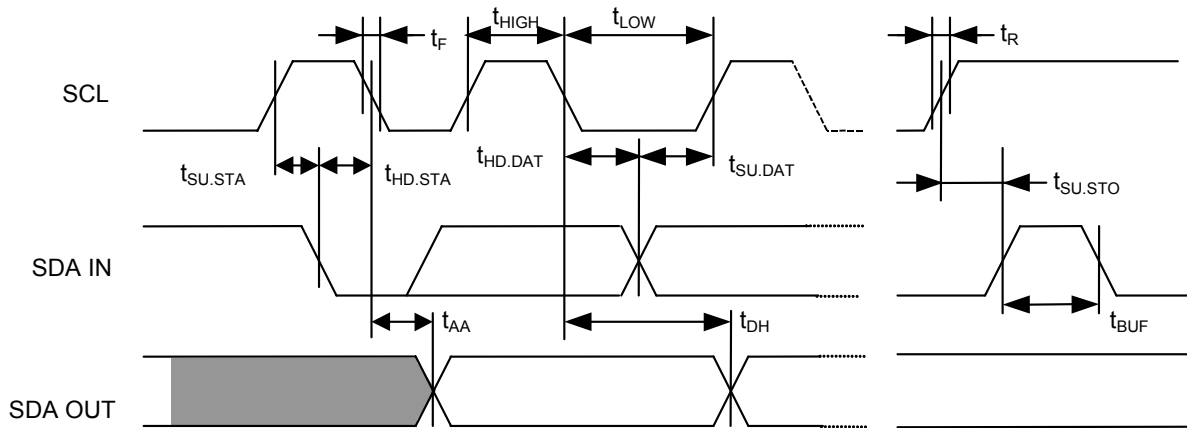
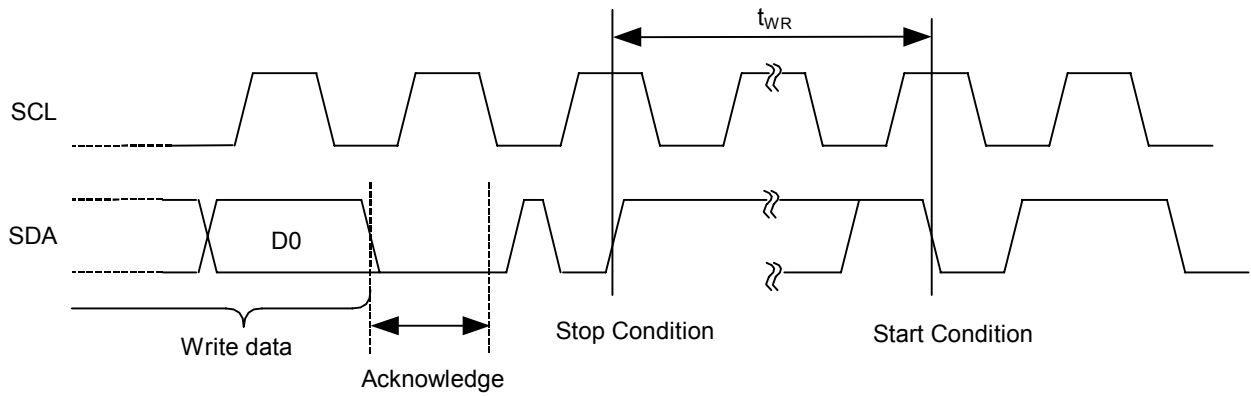


Figure 6 Bus Timing

**Table 12**

Item	Symbol	V <sub>CC</sub> = 2.7 to 5.5 V			Unit
		Min.	Typ.	Max.	
Write time	t <sub>WR</sub>	—	6.0	10.0	ms



**Figure 7 Write Cycle Timing**



## ■ Pin Functions

### 1. Address Input Pins (A0, A1 and A2)

The slave address is assigned by connecting pins A0, A1 and A2 to the GND or to the  $V_{CC}$  respectively. One of the eight different slave address can be assigned by the combination of pins A0, A1 and A2.

The given slave address, which is compared with the slave address transmitted from the master device, is used to select the one among the multiple devices connected to the bus. The address input pin should be connected to the GND or to the  $V_{CC}$ .

### 2. SDA (Serial Data Input / Output) Pin

The SDA pin is used for bi-directional transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.

The SDA line is usually pulled up to the  $V_{CC}$ , and OR-wired with other open-drain or open-collector output devices.

### 3. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rising time and falling time to conform to the specifications.

### 4. WP Pin

The write protection is enabled by connecting the WP pin to the  $V_{CC}$ . When there is no need for write protection, connect the pin to the GND.

## ■ Operation

### 1. Start Condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high. Every operation begins from a start condition.

### 2. Stop Condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high. When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode. When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the E<sup>2</sup>PROM initiates a write cycle.

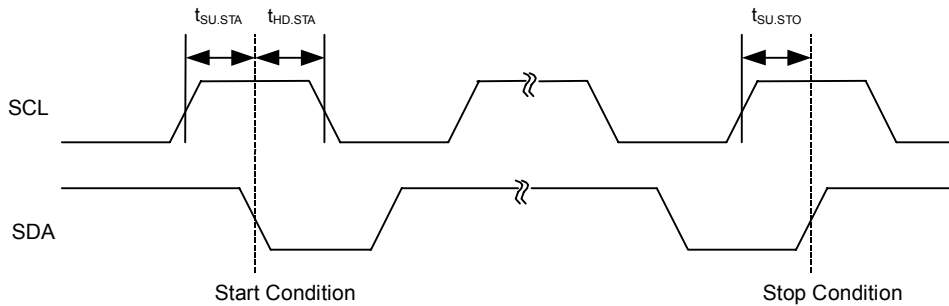
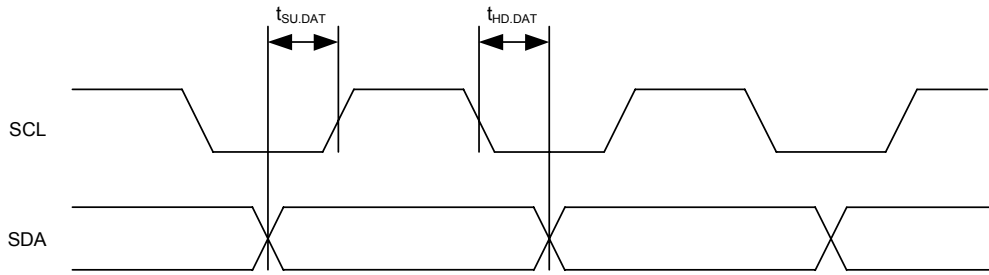


Figure 8 Start / Stop Conditions

**3. Data Transmission**

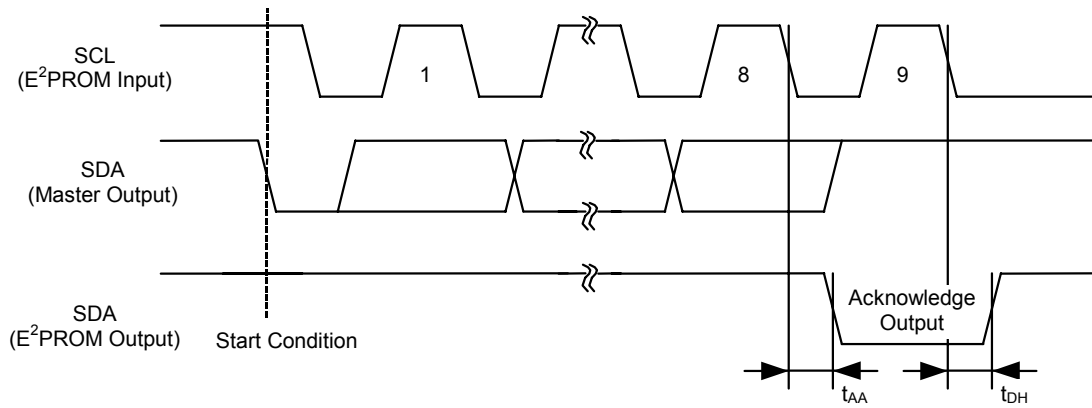
Changing the SDA line while the SCL line is low, data is transmitted.  
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.



**Figure 9 Data Transmission Timing**

**4. Acknowledge**

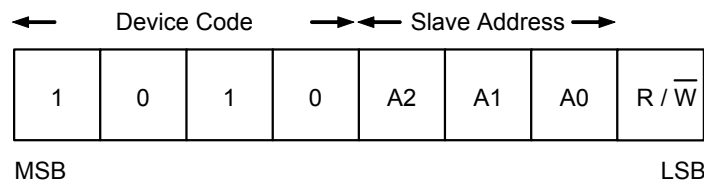
The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.  
When a internal write cycle is in progress, the device does not generate an acknowledge.



**Figure 10 Acknowledge Output Timing**

**5. Device Addressing**

To start communication, the master device on the system generates a start condition to the bus line. Next, the master device sends 7-bit device address and a 1-bit read / write instruction code on to the SDA bus. The 4 most significant bits of the device address are called the "Device Code", and are fixed to "1010". Successive 3 bits are called the "Slave Address". These 3 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A0, A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.



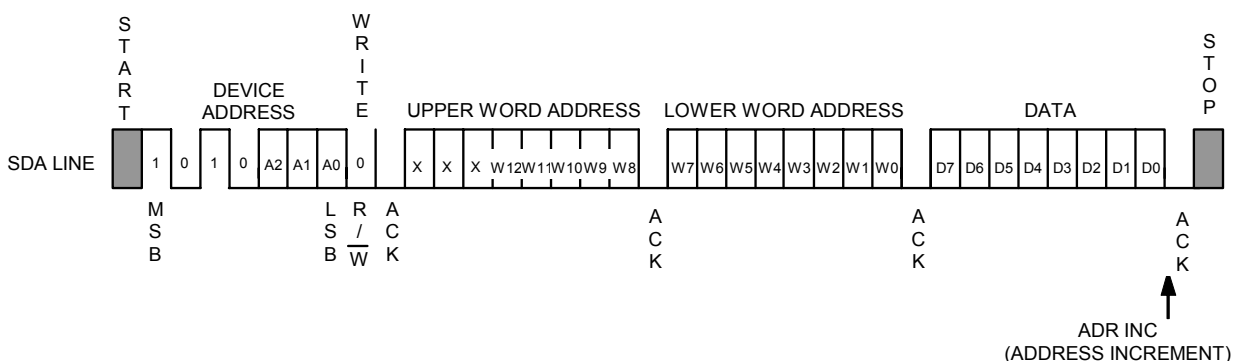
**Figure 11 Device Address**

**6. Write**

**6.1 Byte Write**

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, the E<sup>2</sup>PROM acknowledges it. The E<sup>2</sup>PROM then receives the upper 8 bits of the word address and responds with an acknowledge. And the E<sup>2</sup>PROM receives the lower 8 bits of the word address and responds with an acknowledge. After the E<sup>2</sup>PROM receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.

During the write cycle all operations are forbidden and no acknowledge is generated.



**Figure 12 Byte Write**

6.2 Page Write

The page write mode allows up to 32 bytes to be written in a single wire operation in the S-24CS64A. Basic data transmission procedure is the same as that in the “Byte Write”. However, when the E<sup>2</sup>PROM receives 8-bit write data which corresponds to the page size, the page can be written. When the E<sup>2</sup>PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “0”, following a start condition, it generates an acknowledge. Then the E<sup>2</sup>PROM receives the upper 8 bits of the word address and responds with an acknowledge. And the E<sup>2</sup>PROM receives the lower 8 bits of the word address and responds with an acknowledge. After the E<sup>2</sup>PROM receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The E<sup>2</sup>PROM repeats reception of 8-bit write data and generation of acknowledge in succession. The E<sup>2</sup>PROM can receive as many write data as the maximum page size. Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.

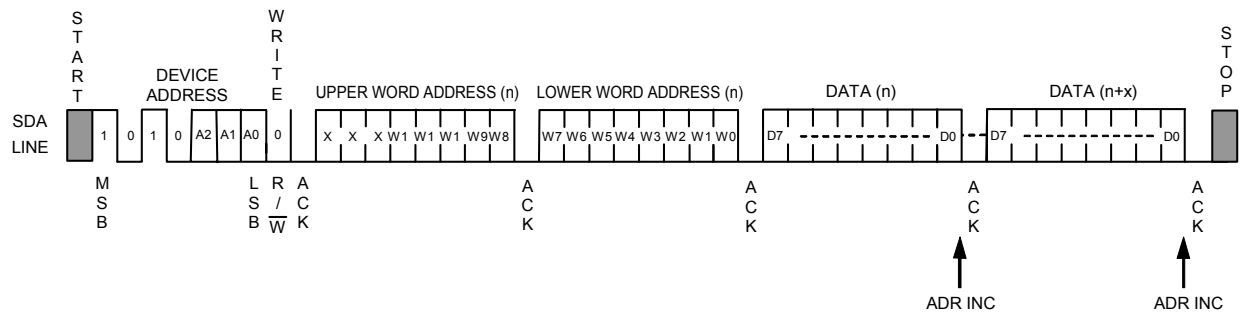


Figure 13 Page Write

The lower 5 bits of the word address are automatically incremented every time when the E<sup>2</sup>PROM receives 8-bit write data. If the size of the write data exceeds 32 bytes, the upper 8 bits of the word address remain unchanged, and the lower 5 bits are rolled over and previously received data will be overwritten.

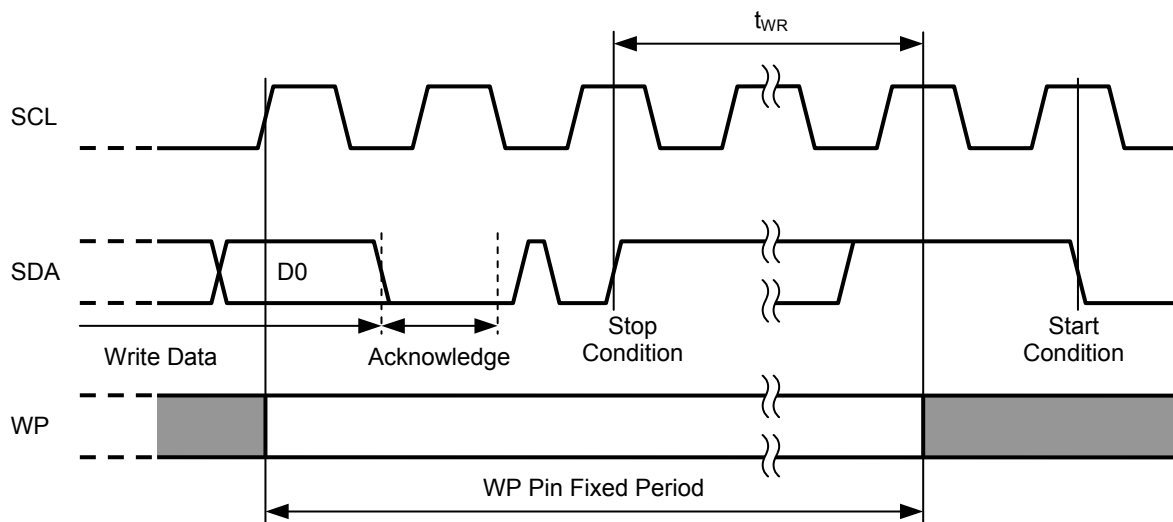
### 6.3 Write Protection

Write protection is available in the S-24CS64A. When the WP pin is connected to the V<sub>CC</sub>, write operation to memory area is forbidden at all.

When the WP pin is connected to the GND, the write protection is invalid, and write operation in all memory area is available.

Fix the level of the WP pin from the rising edge of SCL for loading the last write data (D0) until the end of the write time (10 ms max.). If the WP pin changes during this time, the address data being written at this time is not guaranteed.

There is no need for using write protection, the WP pin should be connected to the GND. The write protection is valid in the operating voltage range.



**Figure 14 WP Pin Fixed Period**

### 6.4 Acknowledge Polling

Acknowledge polling is used to know the completion of the write cycle in the E<sup>2</sup>PROM.

After the E<sup>2</sup>PROM receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.

Accordingly the master device can recognize the completion of the write cycle in the E<sup>2</sup>PROM by detecting a response from the slave device after transmitting the start condition, the device address and the read/write instruction code to the E<sup>2</sup>PROM, namely to the slave devices.

That is, if the E<sup>2</sup>PROM does not generate an acknowledge, the write cycle is in progress and if the E<sup>2</sup>PROM generates an acknowledge, the write cycle has been completed.

Keep the level of the WP pin fixed until acknowledge is confirmed.

It is recommended to use the read instruction "1" as the read/write instruction code transmitted by the master device.

7. Read

7.1 Current Address Read

Either in writing or in reading the E<sup>2</sup>PROM holds the last accessed memory address, internally incremented by one. The memory address is maintained as long as the power voltage is higher than the current address hold voltage V<sub>AH</sub>.

The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the E<sup>2</sup>PROM. This is called "Current Address Read".

In the following the address counter in the E<sup>2</sup>PROM is assumed to be "n".

When the E<sup>2</sup>PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge.

Next an 8-bit data at the address "n" is sent from the E<sup>2</sup>PROM synchronous to the SCL clock. The address counter is incremented at the falling edge of the SCL clock for the 8th bit data, and the content of the address counter becomes n+1.

The master device outputs stop condition not an acknowledge, the reading of E<sup>2</sup>PROM is ended.

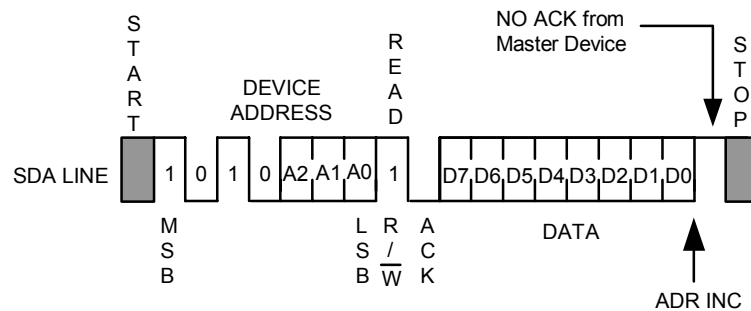


Figure 15 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in the E<sup>2</sup>PROM.

In the read operation the memory address counter in the E<sup>2</sup>PROM is automatically incremented at every falling edge of the SCL clock for the 8th bit of the output data. In the write operation, on the other hand, the upper 8 bits of the memory address are left unchanged and are not incremented at the falling edge of the SCL clock for the 8th bit of the received data.

**7.2 Random Read**

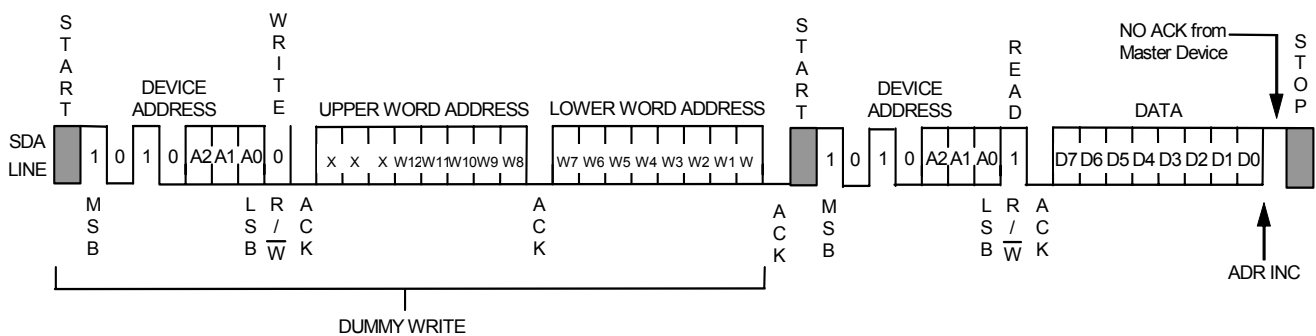
Random read is used to read the data at an arbitrary memory address.

A dummy write is performed to load the memory address into the address counter.

When the E<sup>2</sup>PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “0” following a start condition, it responds with an acknowledge. The E<sup>2</sup>PROM then receives an 8-bit upper word address and responds with an acknowledge. Next the E<sup>2</sup>PROM then receives an 8-bit lower word address and responds with an acknowledge. The memory address is loaded to the address counter in the E<sup>2</sup>PROM by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in a byte write and in a page write.

Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.

That is, when the E<sup>2</sup>PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1”, following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the E<sup>2</sup>PROM in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge, the reading of E<sup>2</sup>PROM is ended.



**Figure 16 Random Read**



7.3 Sequential Read

When the E<sup>2</sup>PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition both in current and random read operations, it responds with an acknowledge. An 8-bit data is then sent from the E<sup>2</sup>PROM synchronous to the SCL clock and the address counter is automatically incremented at the falling edge of the SCL clock for the 8th bit data. When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the E<sup>2</sup>PROM incremented and makes it possible to read data in succession. This is called “Sequential Read”. The master device outputs stop condition not an acknowledge, the reading of E<sup>2</sup>PROM is ended. Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first memory address.

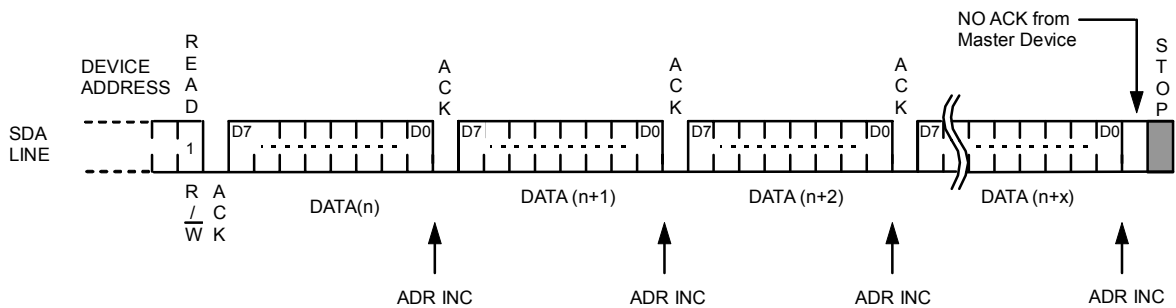


Figure 17 Sequential Read

### 8. Address Increment Timing

The timing for the automatic address increment is the falling edge of the SCL clock for the 8th bit of the read data in read operation and the the falling edge of the SCL clock for the 8th bit of the received data in write operation.

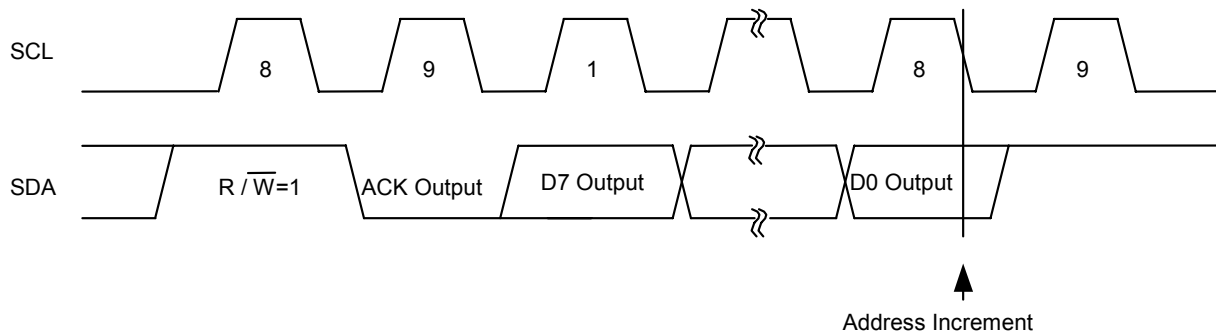


Figure 18 Address Increment Timing in Reading

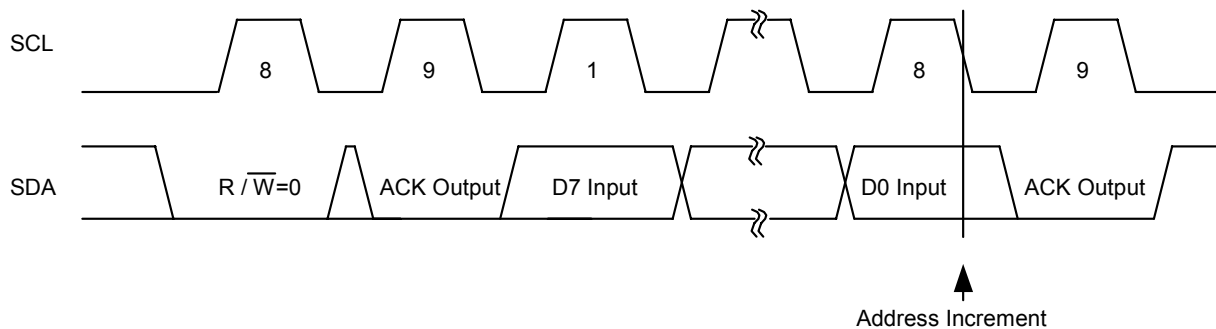


Figure 19 Address Increment Timing in Writing

### Write Inhibition Function at Low Power Voltage

The S-24CS64A have a detection circuit for low power voltage. The detection circuit cancels a write instruction when the power voltage is low or the power switch is on. The detection voltage is 1.85 V typically and the release voltage is 1.95 V typically, the hysteresis of approximate 0.1 V thus exists. (See Figure 20.)

When a low power voltage is detected, a write instruction is canceled at the reception of a stop condition. When the power voltage lowers during a data transmission or a write operation, the date at the address of the operation is not assured.

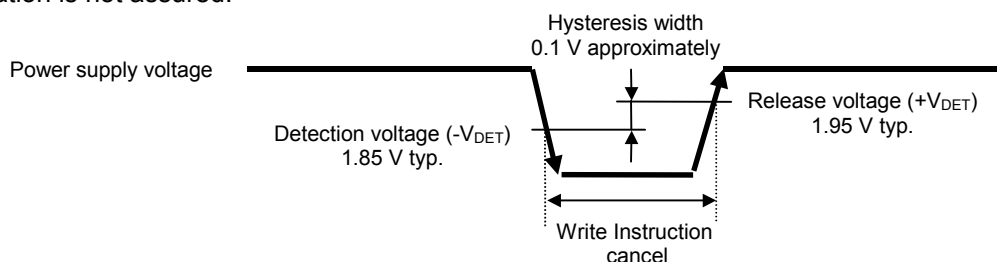


Figure 20 Operation at low power voltage

Seiko Instruments Inc.

## ■ Using S-24CS64A

### 1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

Add a 1 to 5 k $\Omega$  pull-up resistor to the SCL input pin\*<sup>1</sup> and the SDA I/O pin in order to enable the functions of the I<sup>2</sup>C-bus protocol. Normal communication cannot be provided without a pull-up resistor.

- \*1. When the SCL input pin of the E<sup>2</sup>PROM is connected to a tri-state output pin of the microprocessor, connect the same pull-up resistor to prevent a high impedance status from being input to the SCL input pin.

This protects the E<sup>2</sup>PROM from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

### 2. I/O pin equivalent circuit

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.

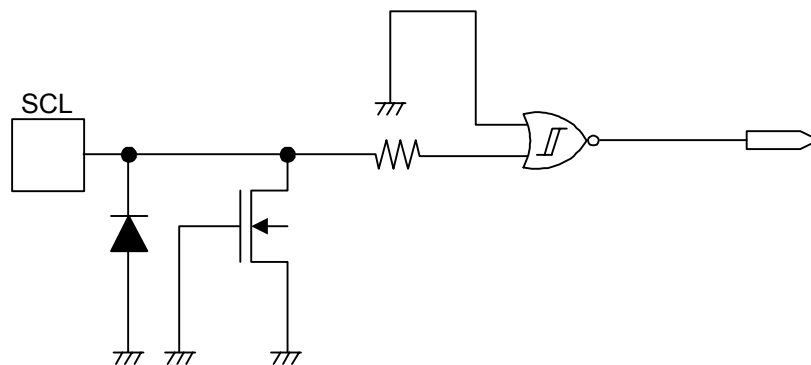


Figure 21 SCL Pin

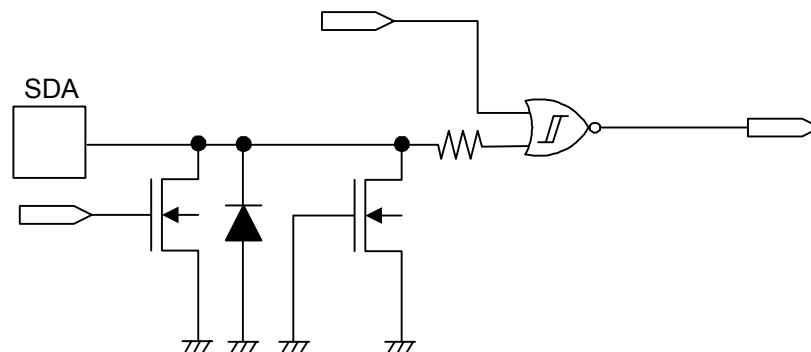


Figure 22 SDA Pin

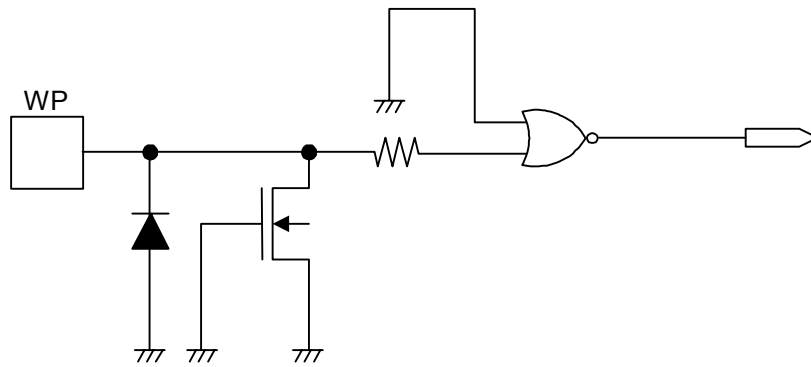


Figure 23 WP Pin

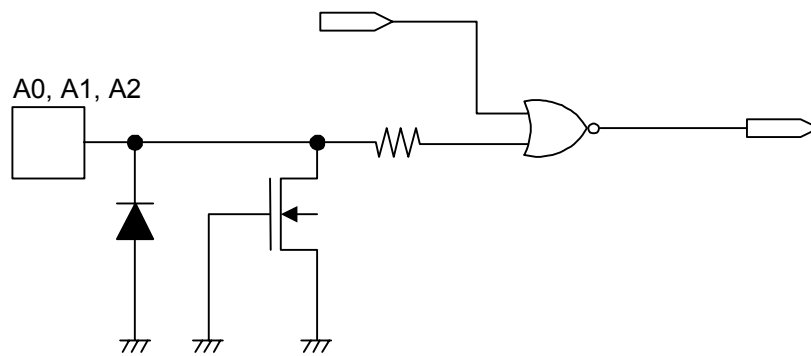


Figure 24 A0, A1, A2 Pin

### 3. Matching phases while E<sup>2</sup>PROM is accessed

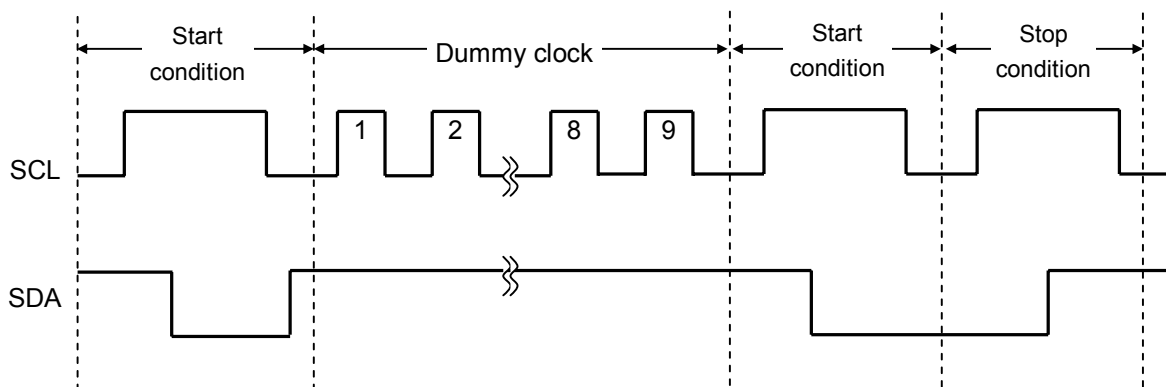
The S-24CS64A does not have a pin for resetting (the internal circuit), therefore, the E<sup>2</sup>PROM cannot be forcibly reset externally. If a communication interruption occurs in the E<sup>2</sup>PROM, it must be reset by software.

For example, even if a reset signal is input to the microprocessor, the internal circuit of the E<sup>2</sup>PROM is not reset as long as the stop condition is not input to the E<sup>2</sup>PROM. In other words, the E<sup>2</sup>PROM retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the E<sup>2</sup>PROM (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

#### [How to reset E<sup>2</sup>PROM]

The E<sup>2</sup>PROM can be reset by the start and stop instructions. When the E<sup>2</sup>PROM is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. **Figure 25** shows this procedure.

First, input the condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the E<sup>2</sup>PROM interrupts the acknowledge output operation or data output, so input the start condition\*<sup>1</sup>. When a start condition is input, the E<sup>2</sup>PROM is reset. To make doubly sure, input the stop condition to the E<sup>2</sup>PROM. Normal operation is then possible.



**Figure 25 Resetting E<sup>2</sup>PROM**

\*1. After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation may be started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

**Remark** It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised.

**4. Acknowledge check**

The I<sup>2</sup>C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the microprocessor and E<sup>2</sup>PROM. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check on the microprocessor side.

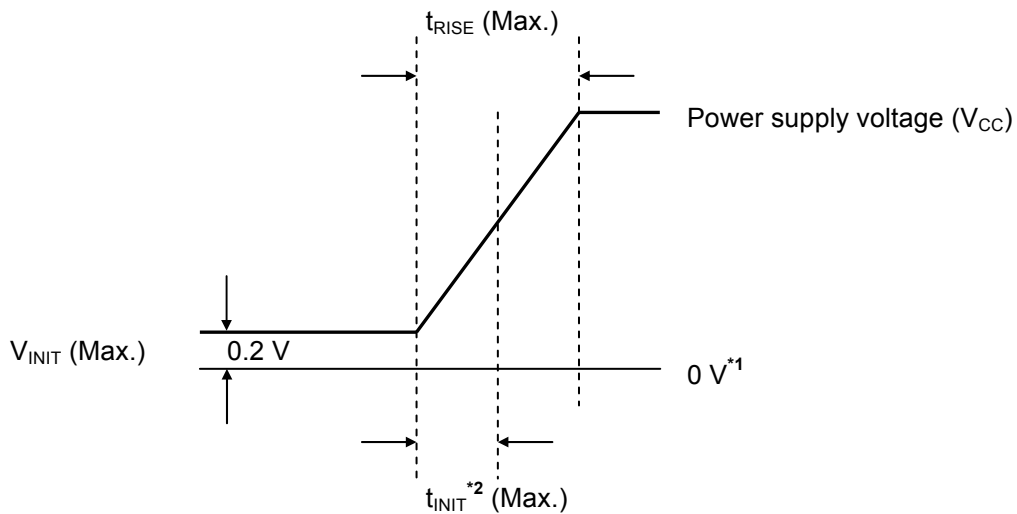
**5. Built-in power-on-clear circuit**

E<sup>2</sup>PROMs have a built-in power-on-clear circuit that initializes the E<sup>2</sup>PROM. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

**5.1 Raising power supply voltage**

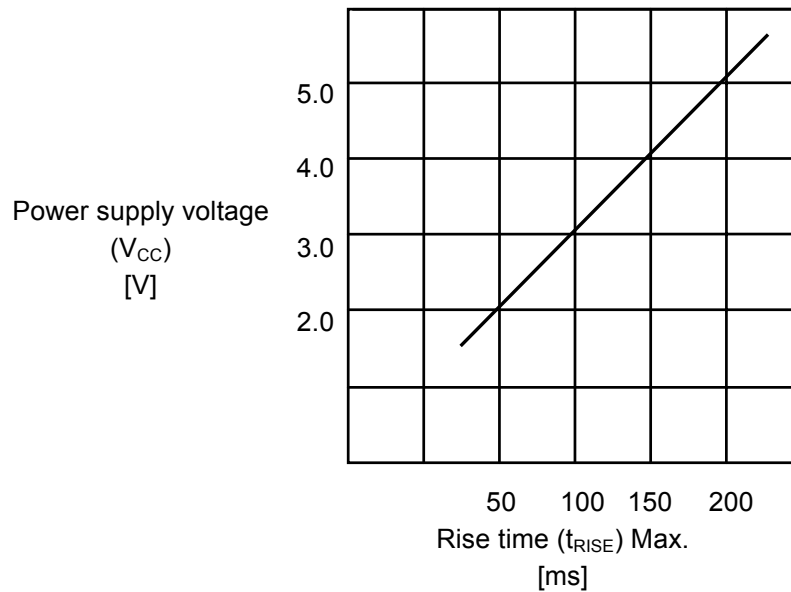
Raise the power supply voltage, starting at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by  $t_{RISE}$  as shown in **Figure 26**.

For example, when the power supply voltage to be used is 5.0 V,  $t_{RISE}$  is 200 ms as shown in **Figure 27**. The power supply voltage must be raised within 200 ms.



- \*1. 0 V means there is no difference in potential between the VCC pin and the GND pin of the E<sup>2</sup>PROM.
- \*2.  $t_{INIT}$  is the time required to initialize the E<sup>2</sup>PROM. No instructions are accepted during this time.

**Figure 26 Raising Power Supply Voltage**



For example:

If your E<sup>2</sup>PROM supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

**Figure 27 Raising Time of Power Supply Voltage**

When initialization is successfully completed via the power-on-clear circuit, the E<sup>2</sup>PROM enters the standby status.

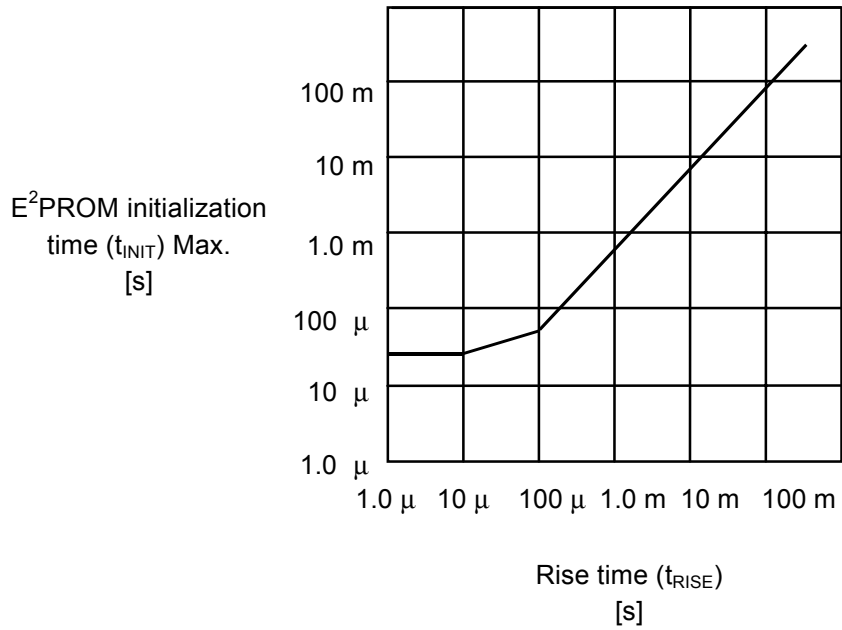
If the power-on-clear circuit does not operate, the following are the possible causes.

- (1) Because the E<sup>2</sup>PROM has not been initialized, an instruction formerly input is valid or an instruction may be inappropriately recognized. In this case, writing may be performed.
- (2) The voltage may have dropped due to power off while the E<sup>2</sup>PROM is being accessed. Even if the microprocessor is reset due to the low power voltage, the E<sup>2</sup>PROM may malfunction unless the power-on-clear operation conditions of E<sup>2</sup>PROM are satisfied. For the power-on-clear operation conditions of E<sup>2</sup>PROM, refer to **5.1 Raising power supply voltage**.

If the power-on-clear circuit does not operate, match the phase (reset) so that the internal E<sup>2</sup>PROM circuit is normally reset. The statuses of the E<sup>2</sup>PROM immediately after the power-on-clear circuit operates and when phase is matched (reset) are the same.

5.2 Wait for the initialization sequence to end

The E<sup>2</sup>PROM executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relationship between the initialization time ( $t_{INIT}$ ) and rise time ( $t_{RISE}$ ) is shown in **Figure 28**.

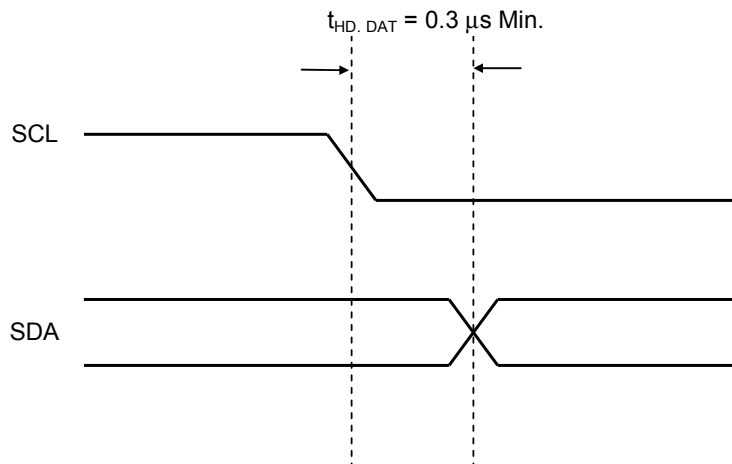


**Figure 28 Initialization Time of E<sup>2</sup>PROM**



**6. Data hold time ( $t_{HD, DAT} = 0 \text{ ns}$ )**

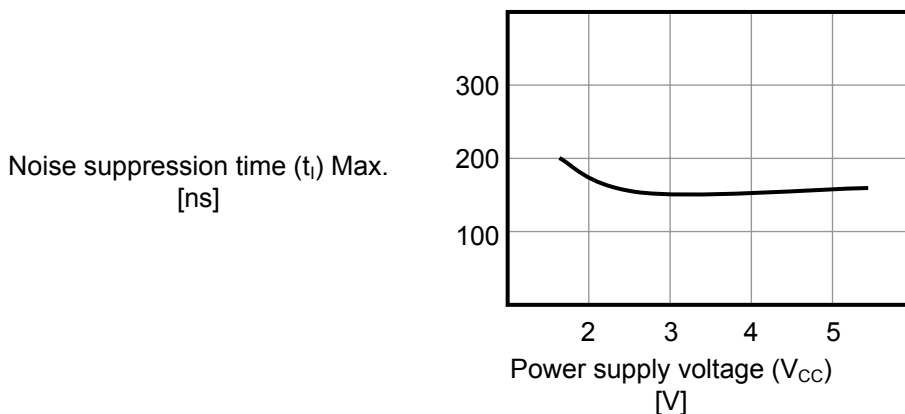
If SCL and SDA of the E<sup>2</sup>PROM are changed at the same time, it is necessary to prevent the start/stop condition from being mistakenly recognized due to the effect of noise. If a start/stop condition is mistakenly recognized during communication, the E<sup>2</sup>PROM enters the standby status. It is recommended that SDA is delayed from the falling edge of SCL by 0.3  $\mu\text{s}$  minimum in the S-24CS64A. This is to prevent time lag caused by the load of the bus line from generating the stop (or start) condition.



**Figure 29 E<sup>2</sup>PROM Data Hold Time**

**7. SDA pin and SCL pin noise suppression time**

The S-24CS64A includes a built-in low-pass filter to suppress noise at the SDA and SCL pins. This means that if the power supply voltage is 5.0 V, noise with a pulse width of 160 ns or less can be suppressed. The guaranteed for details, refer to noise suppression time ( $t_i$ ) in **Table 11**.



**Figure 30 Noise Suppression Time for SDA and SCL Pins**

**8. Trap: E<sup>2</sup>PROM operation in case that the stop condition is received during write operation before receiving the defined data value (less than 8-bit) to SCL pin**

When the E<sup>2</sup>PROM receives the stop condition signal compulsorily, during receiving 1 byte of write data, “write” operation is aborted.

When the E<sup>2</sup>PROM receives the stop condition signal after receiving 1 byte or more of data for “page write”, 8-bit of data received normally before receiving the stop condition signal can be written.

**9. Trap: E<sup>2</sup>PROM operation and write data in case that write data is input more than defined page size at “page write”**

When write data is input more than defined page size at page write operation, for example, S-24CS64A (which can be executed 32-byte page write) is received data more than 33 byte, 8-bit data of the 33rd byte is over written to the first byte in the same page. Data over the capacity of page address cannot be written.

**10. Trap: Severe environments**

Absolute maximum ratings: Do not operate these ICs in excess of the absolute max ratings, as listed on the data sheet. Exceeding the supply voltage rating can cause latch-up.

Operations with moisture on the E<sup>2</sup>PROM pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the E<sup>2</sup>PROM up from low temperature tank during the evaluation. Be sure that not remain frost on E<sup>2</sup>PROM pin to prevent malfunction by short-circuit.

Also attention should be paid in using on environment, which is easy to dew for the same reason.

**■ Precautions**

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

**■ Precautions for WLP package**

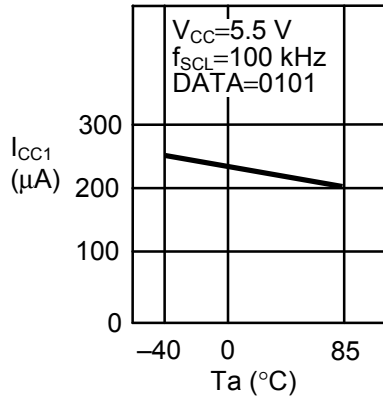
- The side of device silicon substrate is exposed to the marking side of device package. Since this portion has lower strength against the mechanical stress than the standard plastic package, chip, crack, etc should be careful of the handling of a package enough. Moreover, the exposed side of silicon has electrical potential of device substrate, and needs to be kept out of contact with the external potential.
- In this package, the overcoat of the resin of translucence is carried out on the side of device area. Keep it mind that it may affect the characteristic of a device when exposed a device in the bottom of a high light source.

■ Characteristics (Typical Data)

1. DC Characteristics

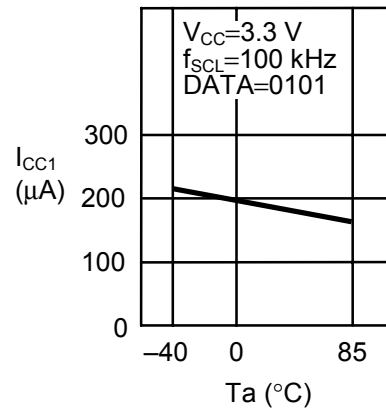
1.1 Current consumption (READ)  $I_{CC1}$

— Ambient temperature  $T_a$



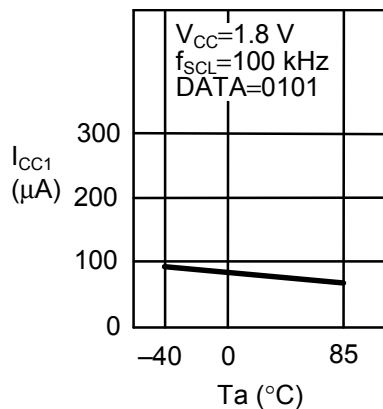
1.2 Current consumption (READ)  $I_{CC1}$

— Ambient temperature  $T_a$



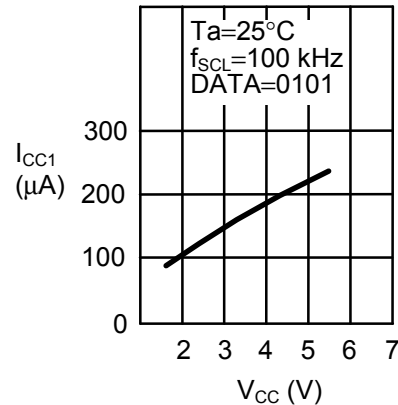
1.3 Current consumption (READ)  $I_{CC1}$

— Ambient temperature  $T_a$



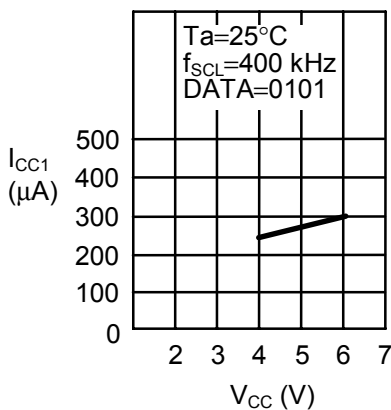
1.4 Current consumption (READ)  $I_{CC1}$

— Power supply voltage  $V_{CC}$



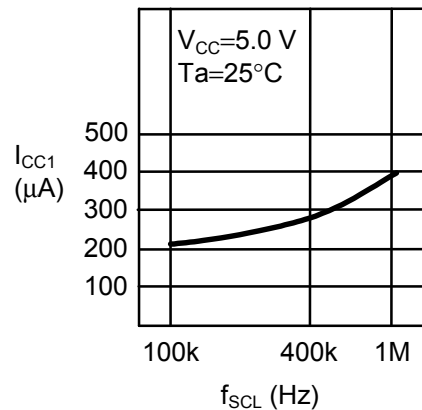
1.5 Current consumption (READ)  $I_{CC1}$

— Power supply voltage  $V_{CC}$

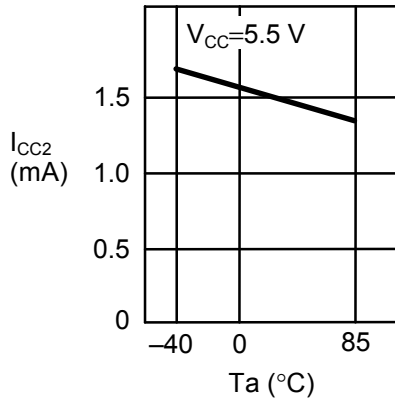


1.6 Current consumption (READ)  $I_{CC1}$

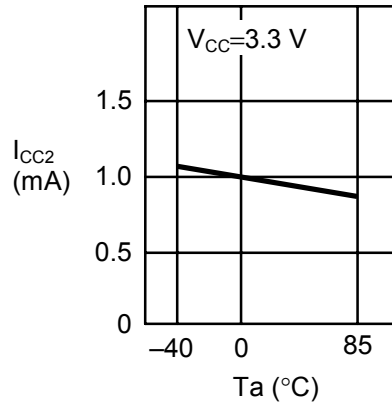
— Clock frequency  $f_{SCL}$



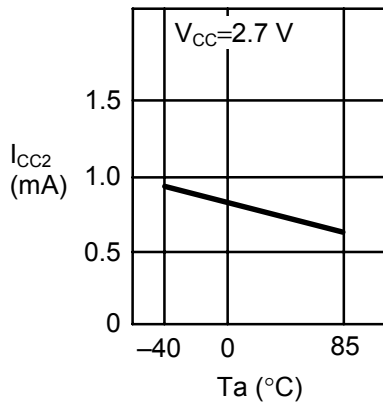
1.7 Current consumption (PROGRAM)  $I_{CC2}$   
— Ambient temperature  $T_a$



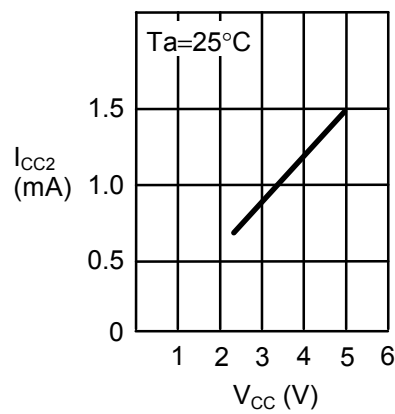
1.8 Current consumption (PROGRAM)  $I_{CC2}$   
— Ambient temperature  $T_a$



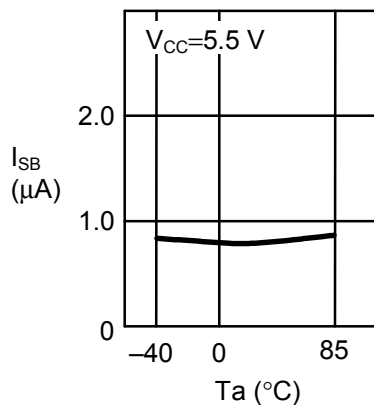
1.9 Current consumption (PROGRAM)  $I_{CC2}$   
— Ambient temperature  $T_a$



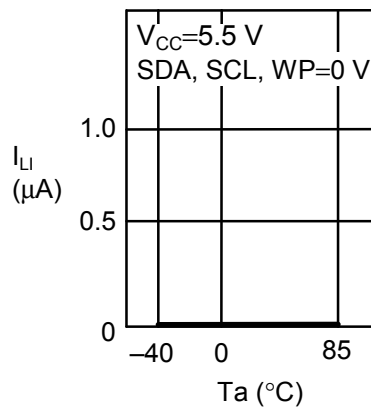
1.10 Current consumption (PROGRAM)  $I_{CC2}$   
— Power supply voltage  $V_{CC}$



1.11 Standby current consumption  $I_{SB}$   
— Ambient temperature  $T_a$

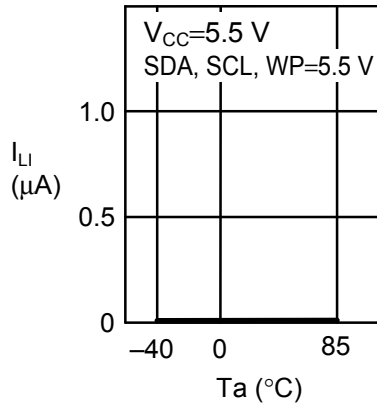


1.12 Input leakage current  $I_{LI}$   
— Ambient temperature  $T_a$



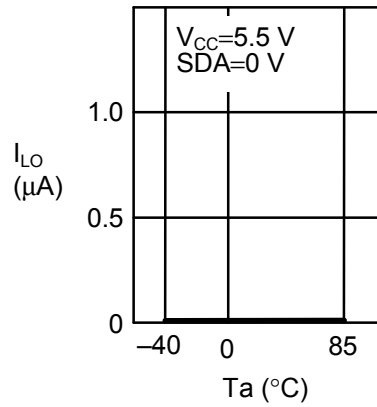
**1.13 Input leakage current  $I_{LI}$**

— Ambient temperature  $T_a$



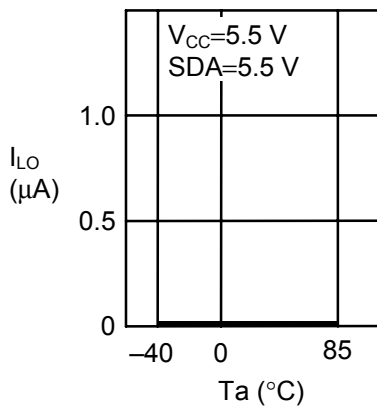
**1.14 Output leakage current  $I_{LO}$**

— Ambient temperature  $T_a$



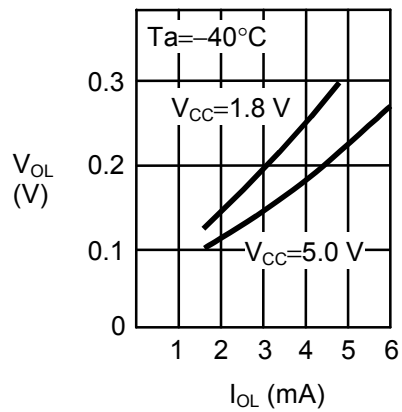
**1.15 Output leakage current  $I_{LO}$**

— Ambient temperature  $T_a$



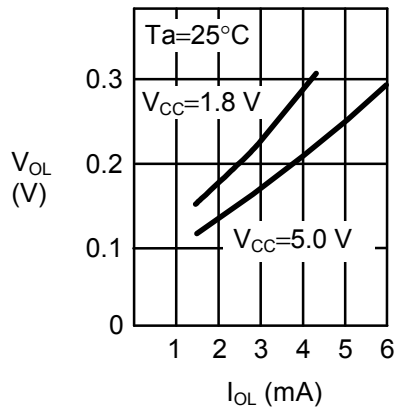
**1.16 Low level output voltage  $V_{OL}$**

— Low level output current  $I_{OL}$



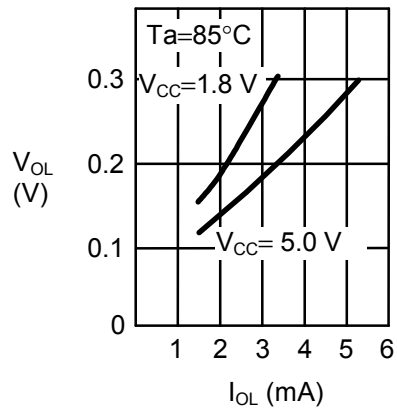
**1.17 Low level output voltage  $V_{OL}$**

— Low level output current  $I_{OL}$



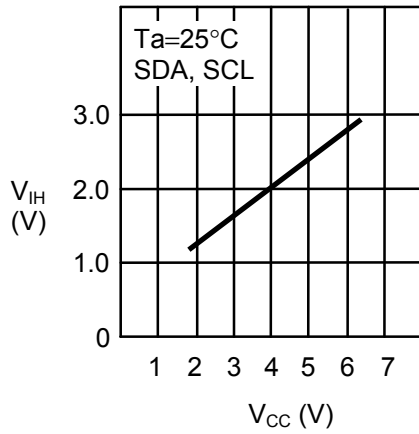
**1.18 Low level output voltage  $V_{OL}$**

— Low level output current  $I_{OL}$



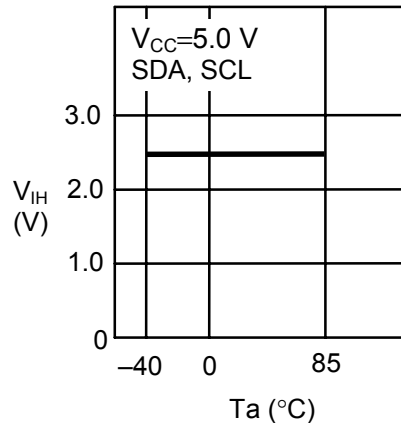
1.19 High input inversion voltage  $V_{IH}$

— Power supply voltage  $V_{CC}$



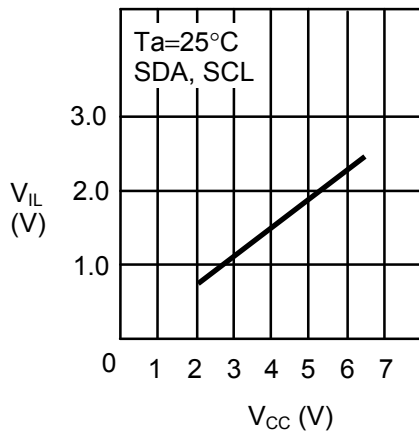
1.20 High input inversion voltage  $V_{IH}$

— Ambient temperature  $T_a$



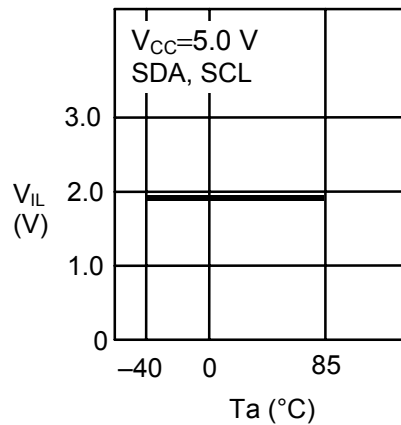
1.21 Low input inversion voltage  $V_{IL}$

— Power supply voltage  $V_{CC}$



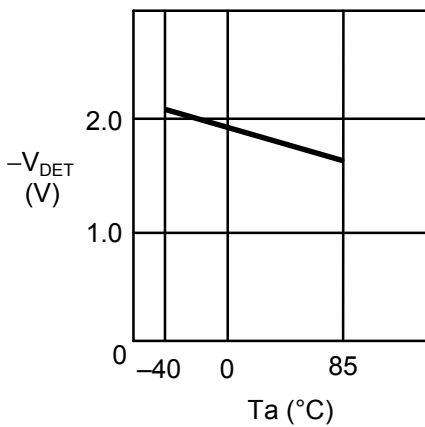
1.22 Low input inversion voltage  $V_{IL}$

— Ambient temperature  $T_a$



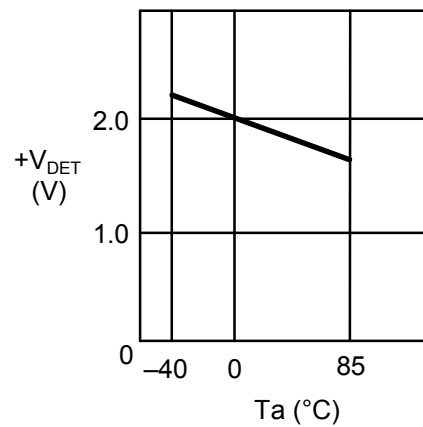
1.23 Low power supply detection voltage  $-V_{DET}$

— Ambient temperature  $T_a$



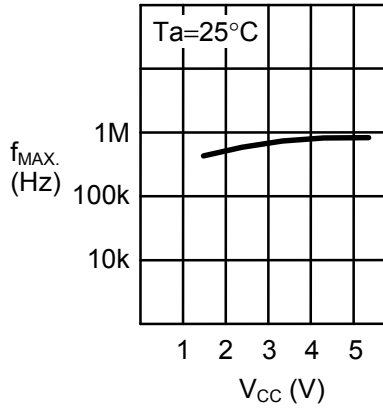
1.24 Low power supply release voltage  $+V_{DET}$

— Ambient temperature  $T_a$

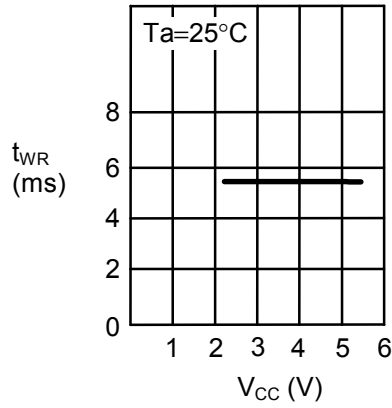


**2. AC Characteristics**

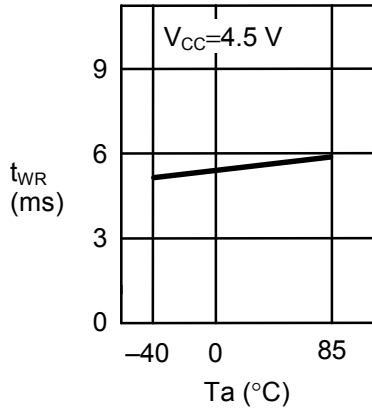
**2.1 Maximum operating frequency  $f_{MAX}$ .  
— Power supply voltage  $V_{CC}$**



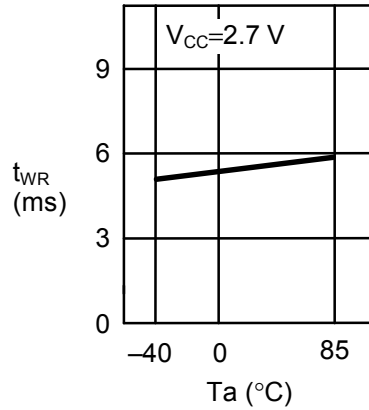
**2.2 Write time  $t_{WR}$ — Power supply voltage  $V_{CC}$**



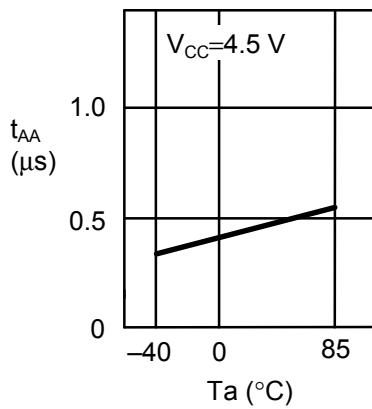
**2.3 Write time  $t_{WR}$ — Ambient temperature  $T_a$**



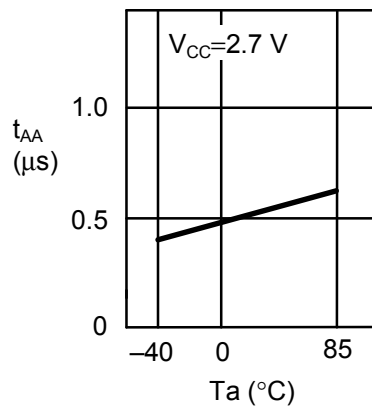
**2.4 Write time  $t_{WR}$ — Ambient temperature  $T_a$**



**2.5 SDA output delay time  $t_{AA}$   
— Ambient temperature  $T_a$**

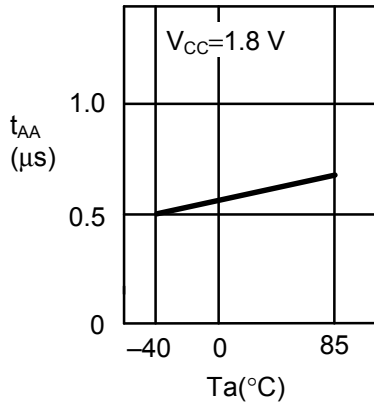


**2.6 SDA output delay time  $t_{AA}$   
— Ambient temperature  $T_a$**



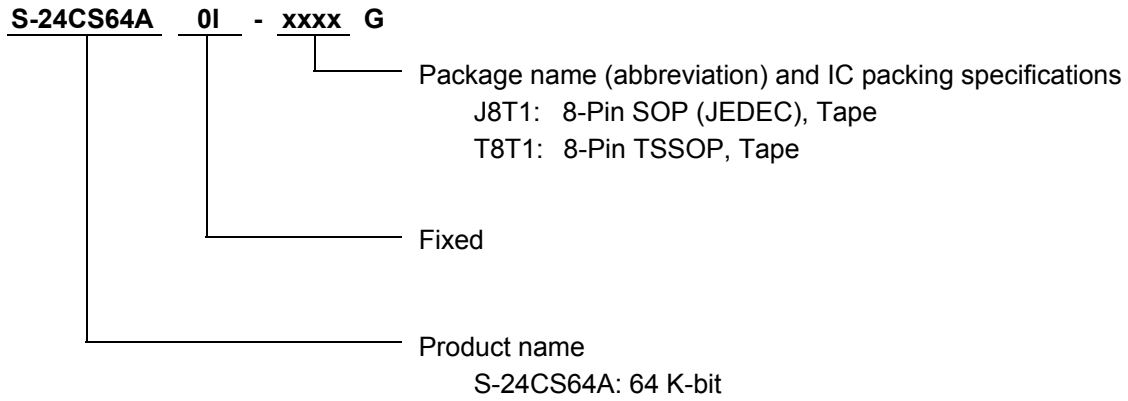


2.7 SDA output delay time  $t_{AA}$   
— Ambient temperature  $T_a$

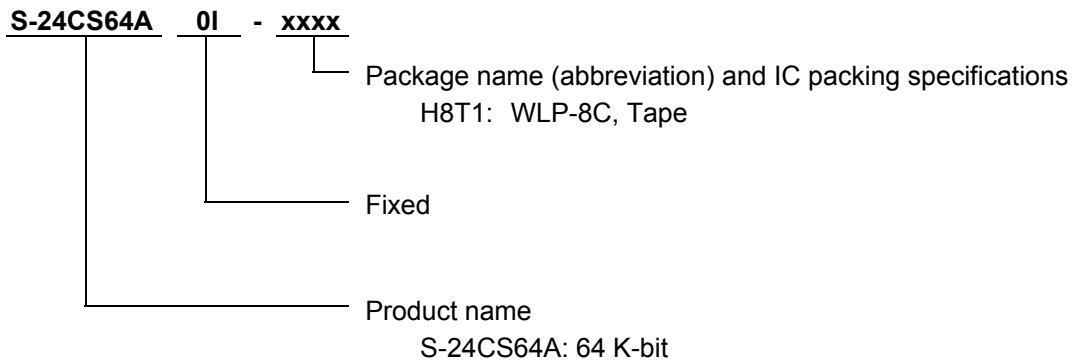


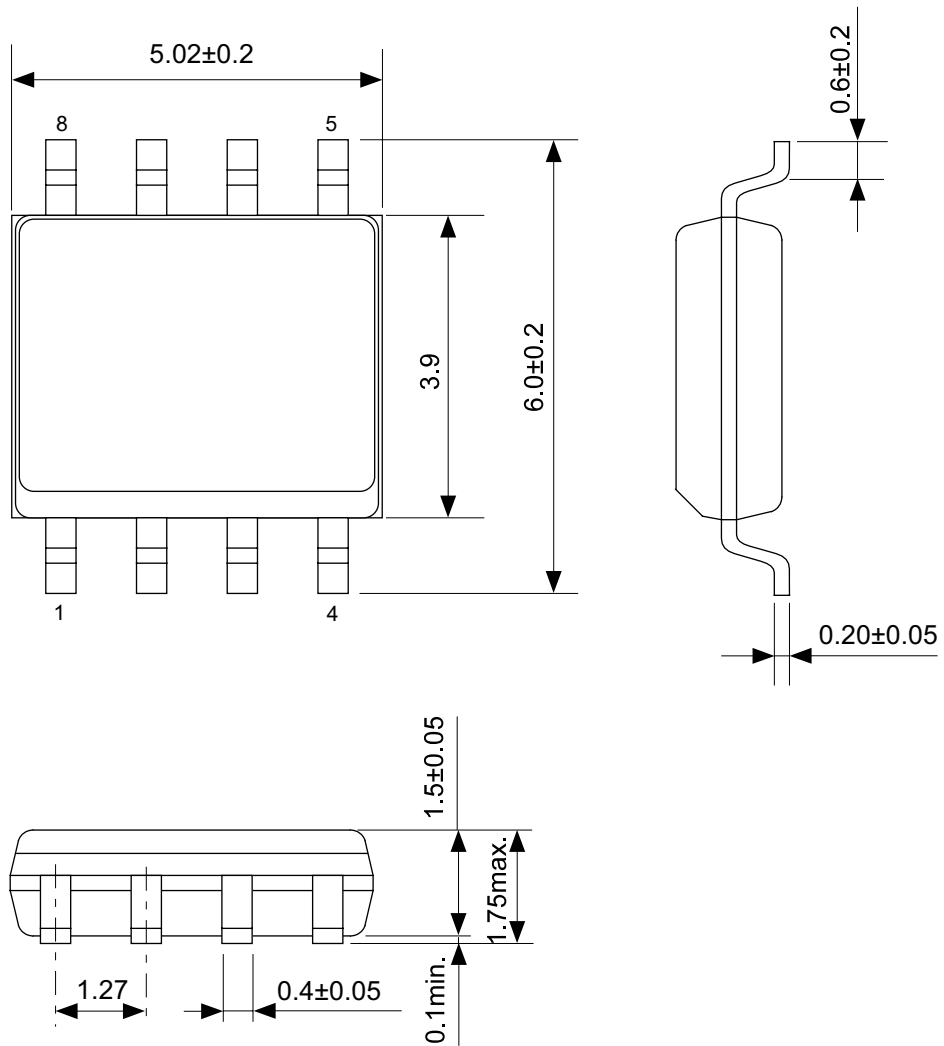
■ Product Name Structure

1. 8-Pin SOP(JEDEC), 8-Pin TSSOP Packages



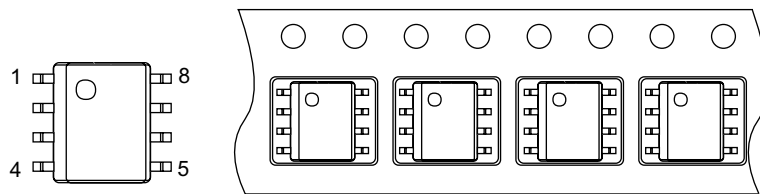
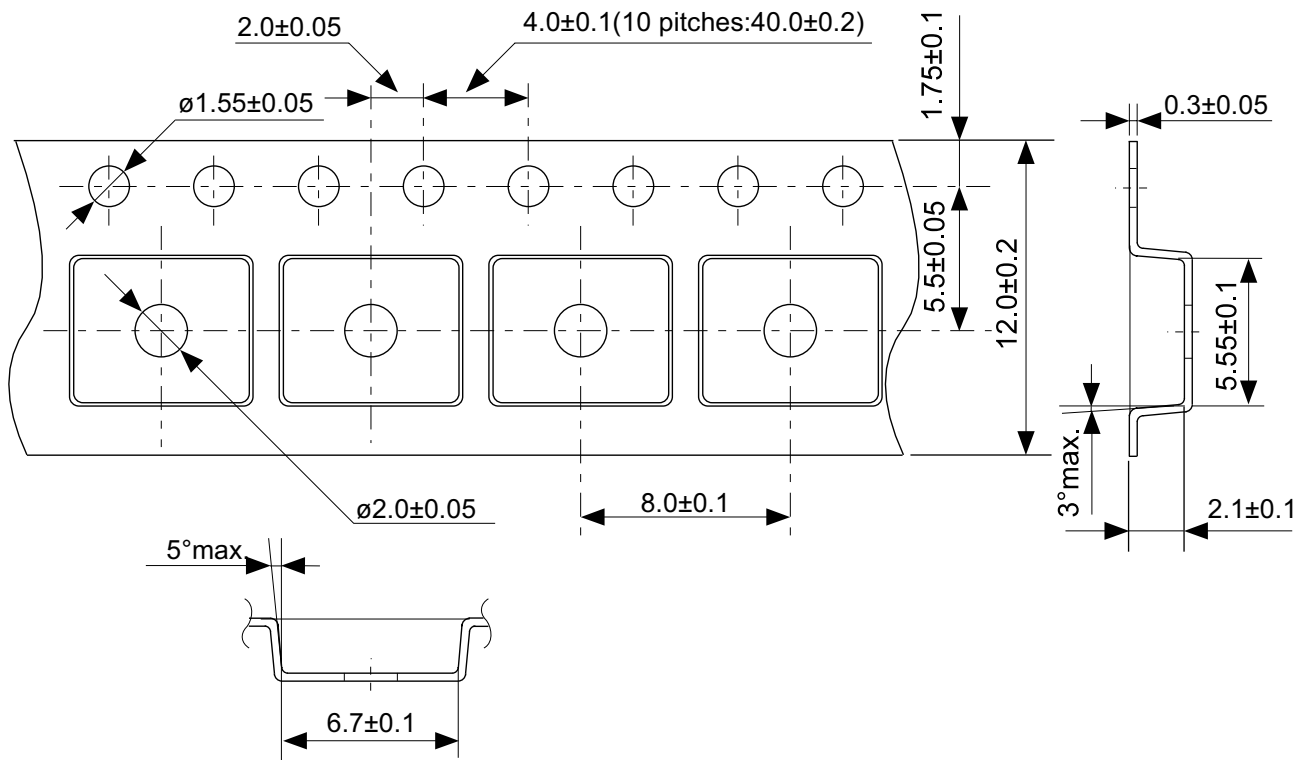
2. WLP-8C Package





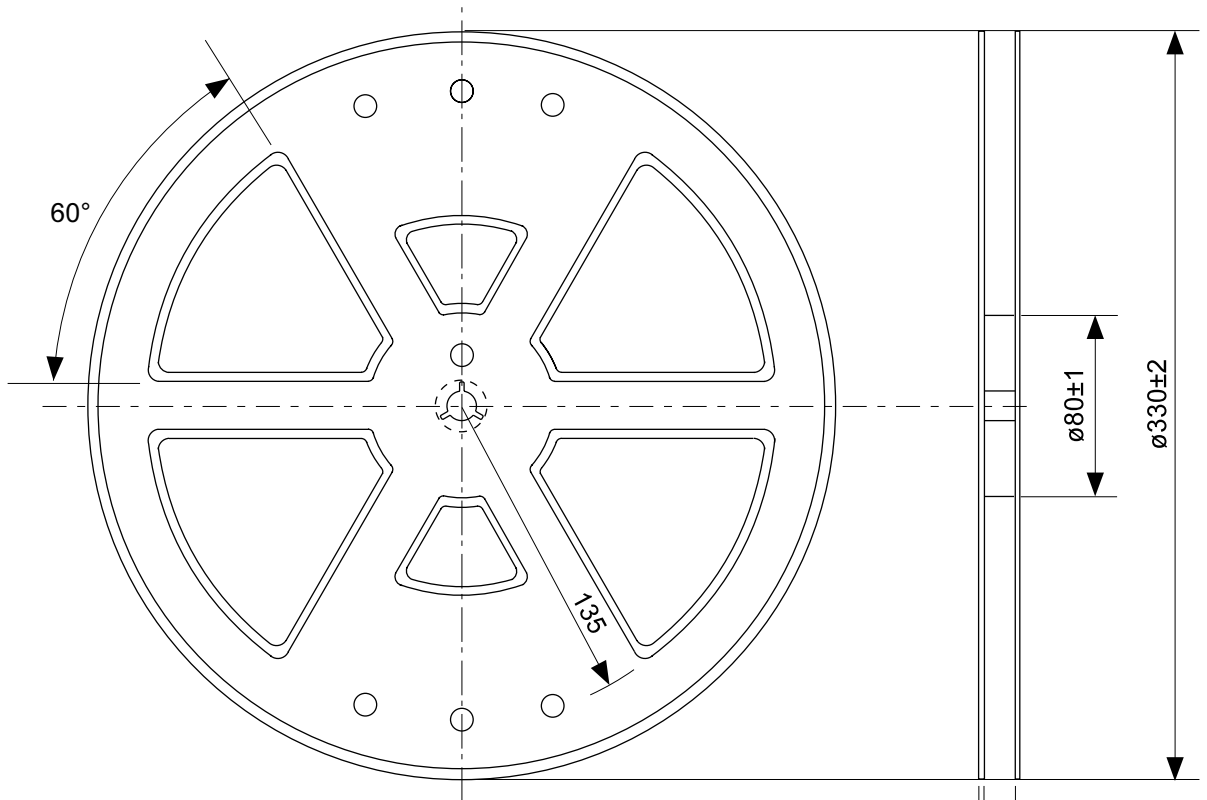
No. FJ008-A-P-SD-2.1

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

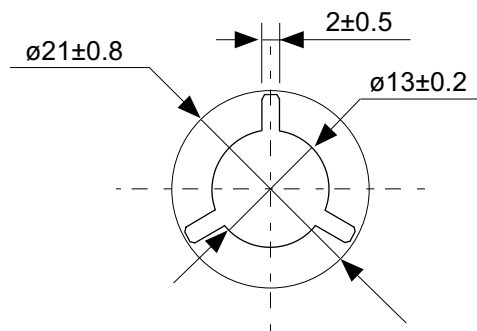


No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

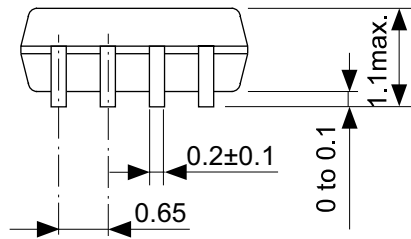
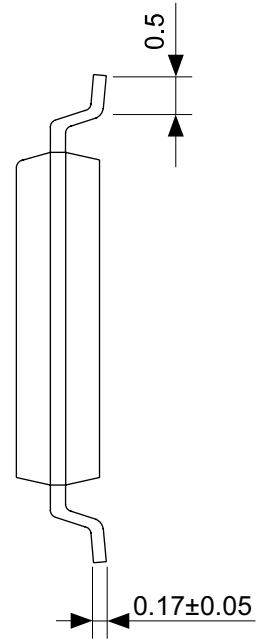
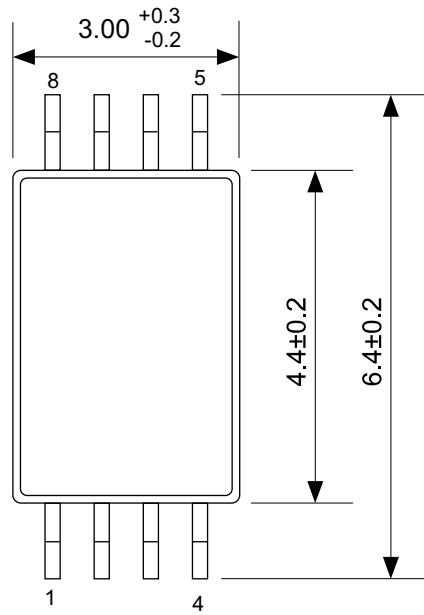


Enlarged drawing in the central part



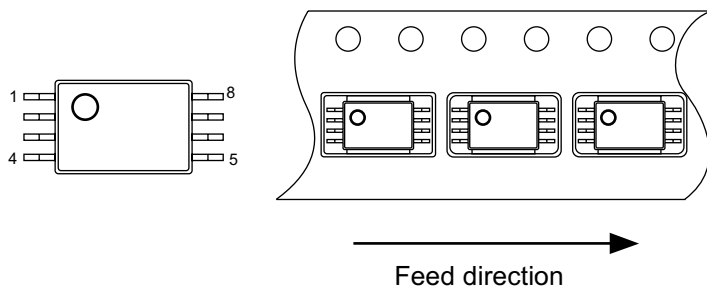
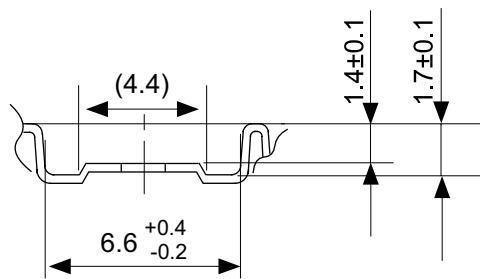
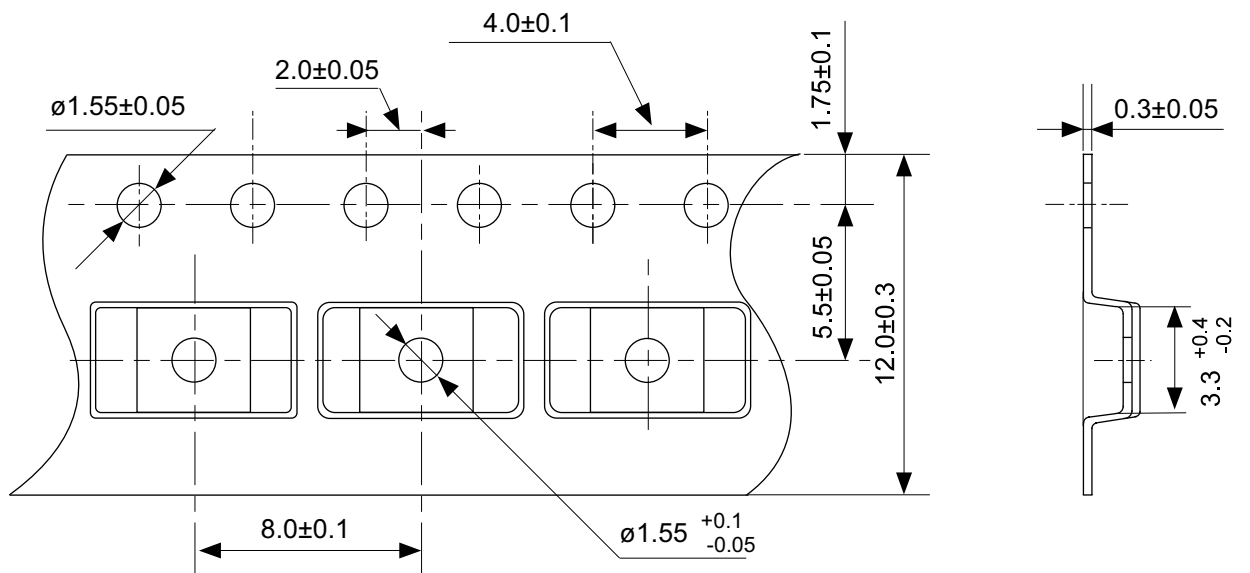
No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			



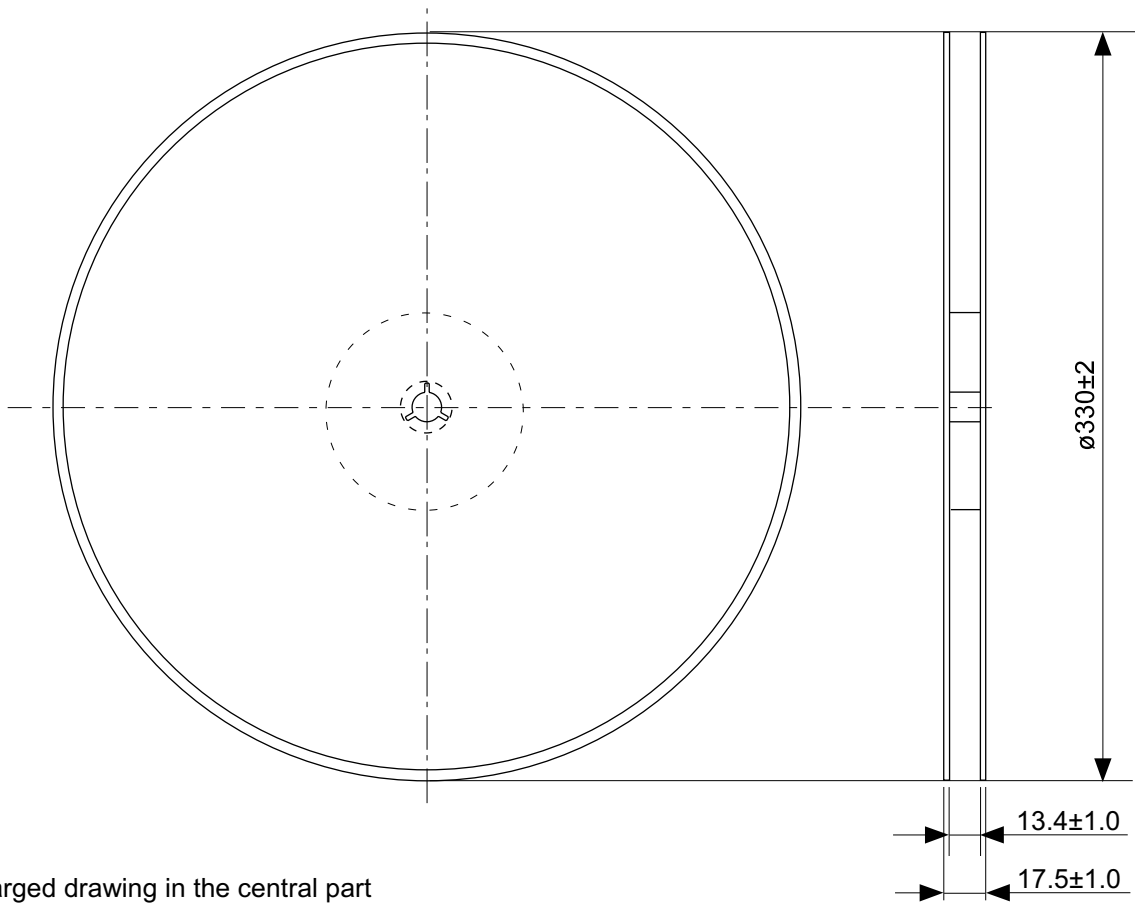
No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

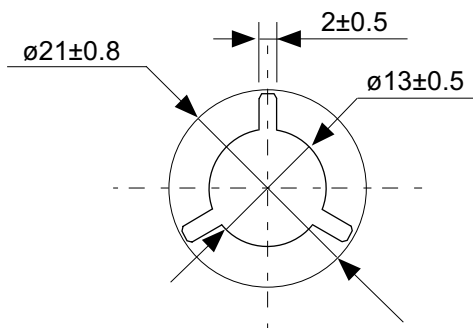


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



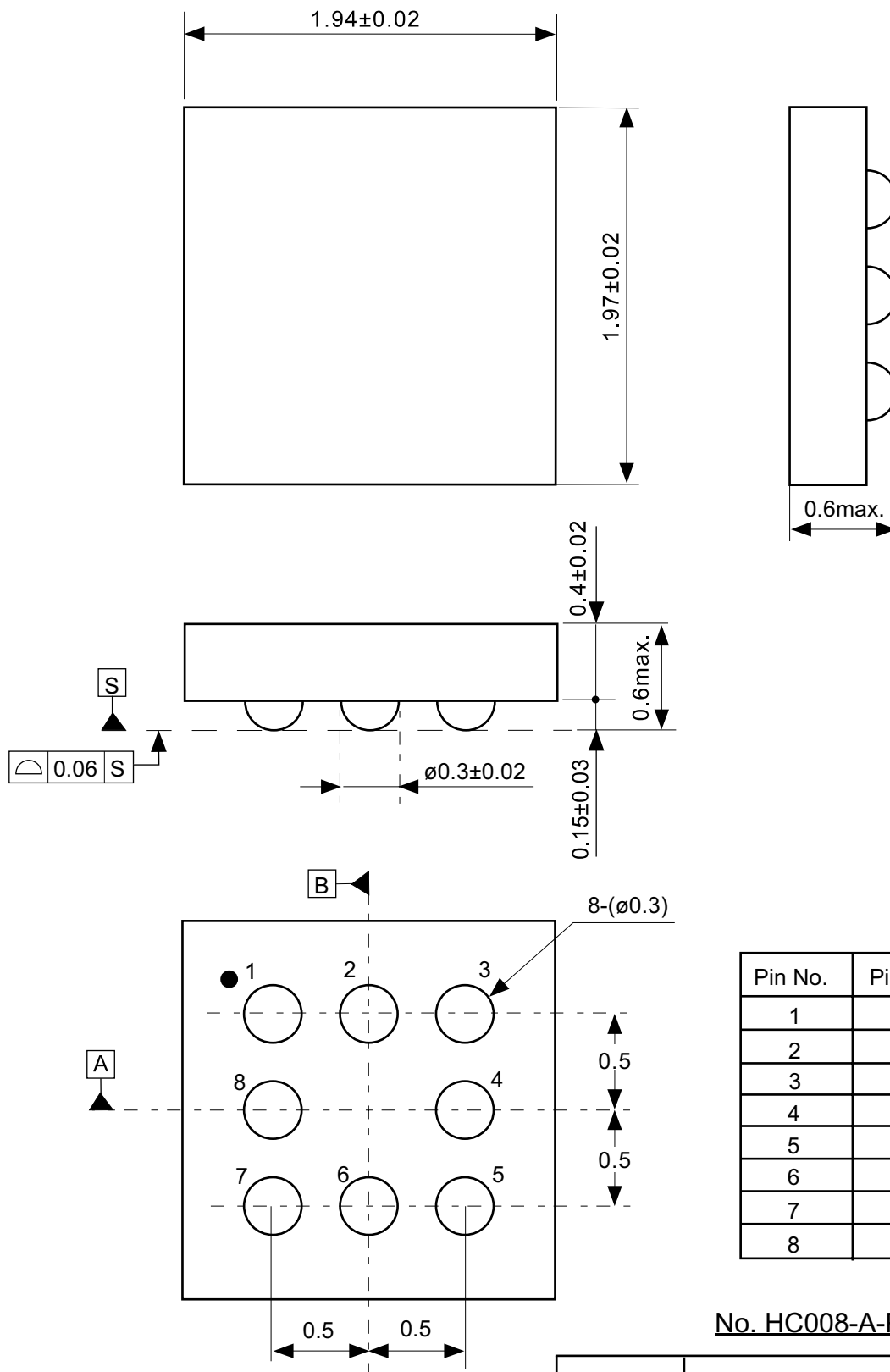
Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			



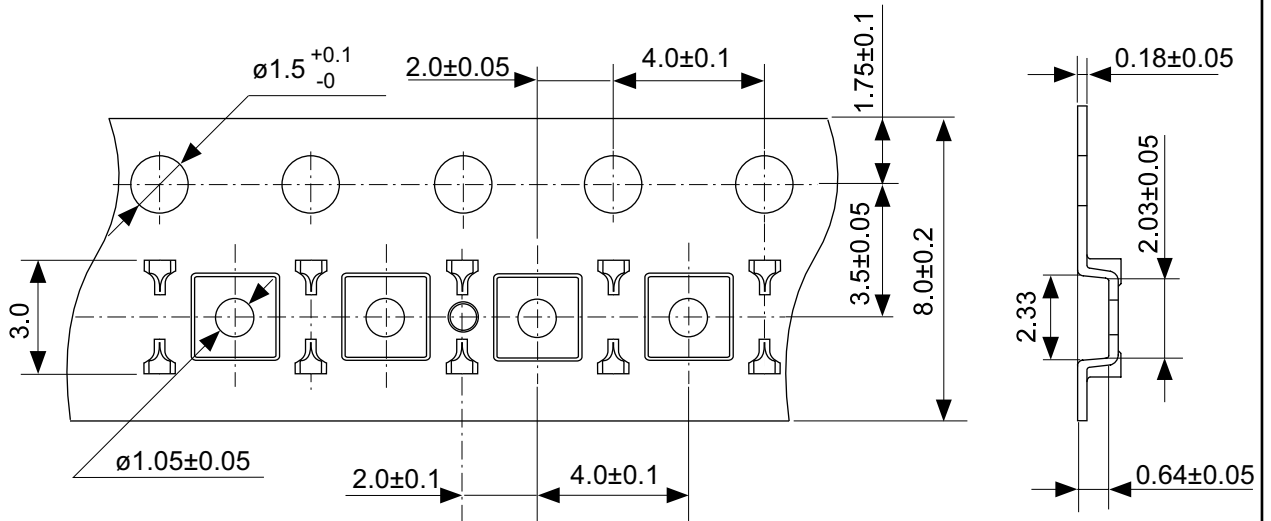


Pin No.	Pin name
1	A0
2	VCC
3	WP
4	SCL
5	SDA
6	GND
7	A2
8	A1

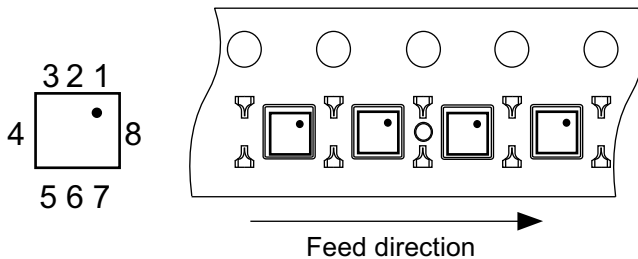
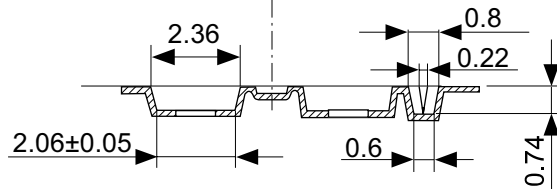
No. HC008-A-P-SD-1.0

TITLE	WLP-8C-A-PKG Dimensions
No.	HC008-A-P-SD-1.0
SCALE	
UNIT	mm

Seiko Instruments Inc.

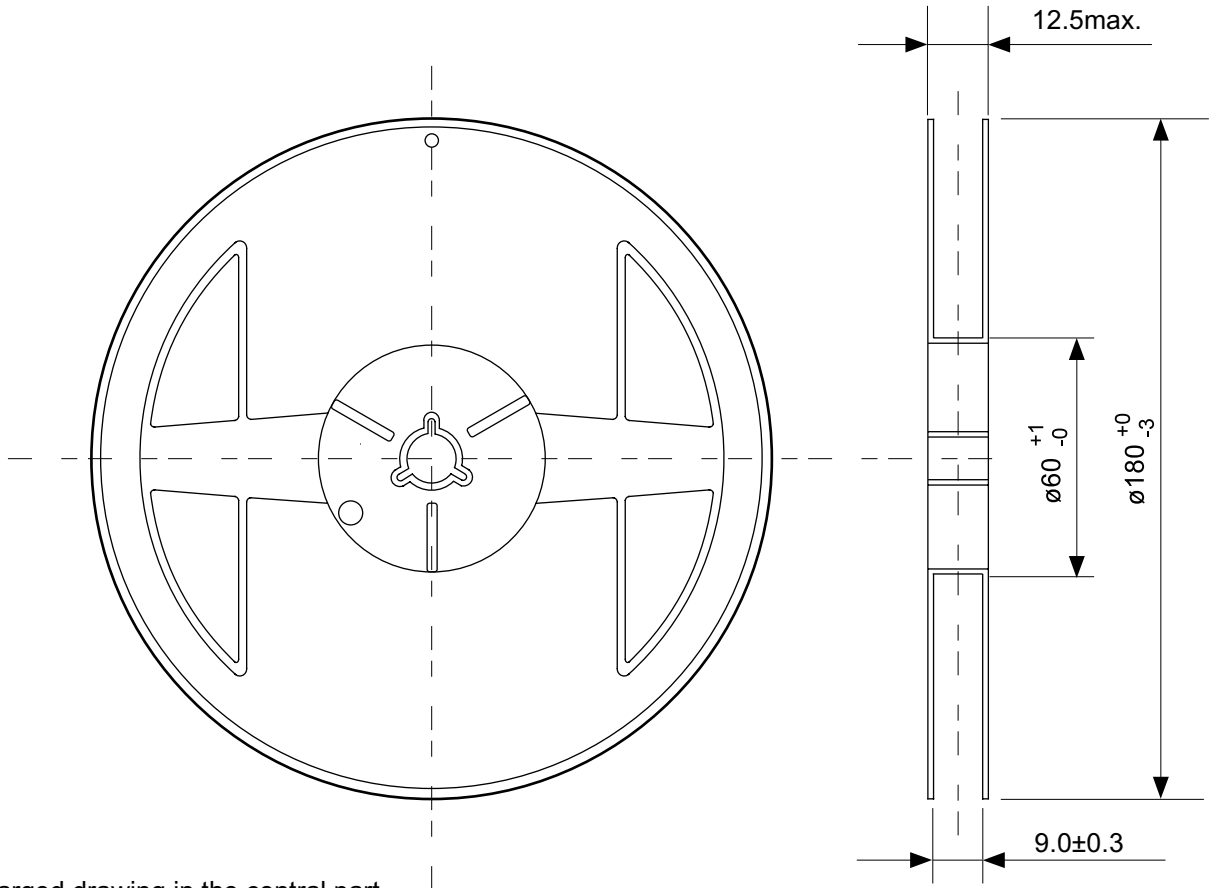


Count mark ( $\phi 0.8$ , Depth 0.2)  
(Every 10 pockets)

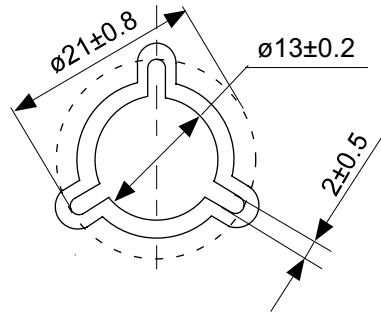


No. HC008-A-C-SD-1.0

TITLE	WLP-8C-A-Carrier Tape
No.	HC008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. HC008-A-R-SD-1.0

TITLE	WLP-8C-A-Reel		
No.	HC008-A-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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